ABSTRACT OF THE DISCLOSURE

A DC-offset eliminating circuit changes a coefficient α for determining a DC-offset follow-up speed. The coefficient α is changed to a smaller value or 0 in a case where a signal showing a detection that a reception is ceased, is received from a signal-end detecting circuit, or in a case where a signal for partly turning off the circuits for the reduction of power consumption is received from a control circuit, if the received frame is not destined for the receiver itself. The circuit remains the coefficient α to a smaller value immediately after the reception is resumed. Additionally, the circuit returns the coefficient α to the normal value in response to the reception of a signal showing that an alignment signal is detected immediately after a preamble portion. The circuit then reduces the DC-offset follow-up speed as much as possible at the time when the preamble portion is received, thereby avoiding the DC-offset deviation caused by the preamble patterns.